CS485xx 3V to 5.5V RS-485 Transceiver with ±20kV ESD Protection

1 Key Features

- Meets or Exceeds the Requirements of the TIA/EIA-485A Standard
- Data Rate
  - CS48505x: 500kbps
  - CS48520x: 20Mbps
- 3V to 5.5V Supply Voltage
- Differential Output Exceeds 2.1 V for PROFIBUS Compatibility with 5-V Supply
- Driver with Current Limiter and Thermal Shutdown Protection
- Bus Pins ESD Protection
  - ±20kV HBM ESD
  - ±4kV IEC 61000-4-2 Contact Discharge
- 1/2 Unit Load (Up to 64 Bus Nodes)
- Open, Short and Idle Bus Failsafe Protection
- Extended Industrial Temperature Range: –40°C to 125°C
- Common Mode Range: –7V to 12V
- Low Standby Current: <5µA
- Glitch-free during Power On and Power Off
- Support Multiple Packages: SOIC8, MSOP8 and DFN8

2 Applications

- Factory Automation & Control
- Smart Meters
- Home and Building Automation
- HVAC
- Video Surveillance
- Wireless Infrastructure

3 Description

The CS485xx is a family of half-duplex RS-485 transceivers which could be used in harsh industrial and electrical environments. The bus pins could withstand high-level ESD events to protect internal circuit without damage.

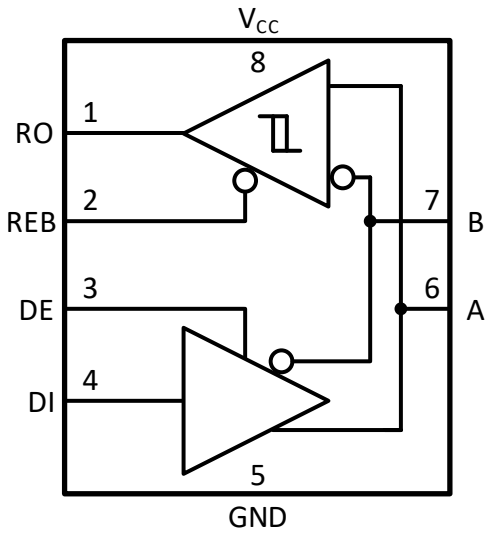
These devices could provide multiple package options including SOIC8, MSOP8 and DFN8, which are suitable for space constrained and long-cable communication applications. Each device contains one driver and one receiver, supporting the power supply range from 3V to 5.5V.

These devices are specified over ambient free-air temperature range of –40°C to 125°C.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CS48505S CS48520S	SOIC8 (S)	4.9mm × 3.9mm
CS48505M CS48520M	MSOP8 (M)	3mm × 3mm
CS48505D CS48520D	DFN8 (D)	3mm × 3mm

Simplified Schematic



4 Ordering Guide

Table 4-1 Ordering Guide for Valid Ordering Part Number

Part Number	Date Rate (Mbps)	Full/Half-Duplex	Package
CS48505S	0.5	Half-Duplex	SOIC8 (S)
CS48520S	20	Half-Duplex	SOIC8 (S)
CS48505M	0.5	Half-Duplex	MSOP8 (M)
CS48520M	20	Half-Duplex	MSOP8 (M)
CS48505D	0.5	Half-Duplex	DFN8 (D)
CS48520D	20	Half-Duplex	DFN8 (D)

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5 Revision History

Revision	Description	Date	Page
Version 1.00	NA	2022/04/28	NA
Version 1.01	1. Update the maximum number of nodes supported by the bus to 64 2. Update the value of bus input current and impedance	2022/05/23	1 6
Version 1.02	1. Update EFT items 2. Add the absolute maximum rated value of the differential voltage between A and B 3. Add testing condition for bus input impedance R_I	2023/08/10	5 5 6
Version 1.03	1. Add descriptions to driver enable time and receiver enable time 2. Modify other items to keep same with Chinese version	2024/04/29	7 All

6 Pin Descriptions and Functions

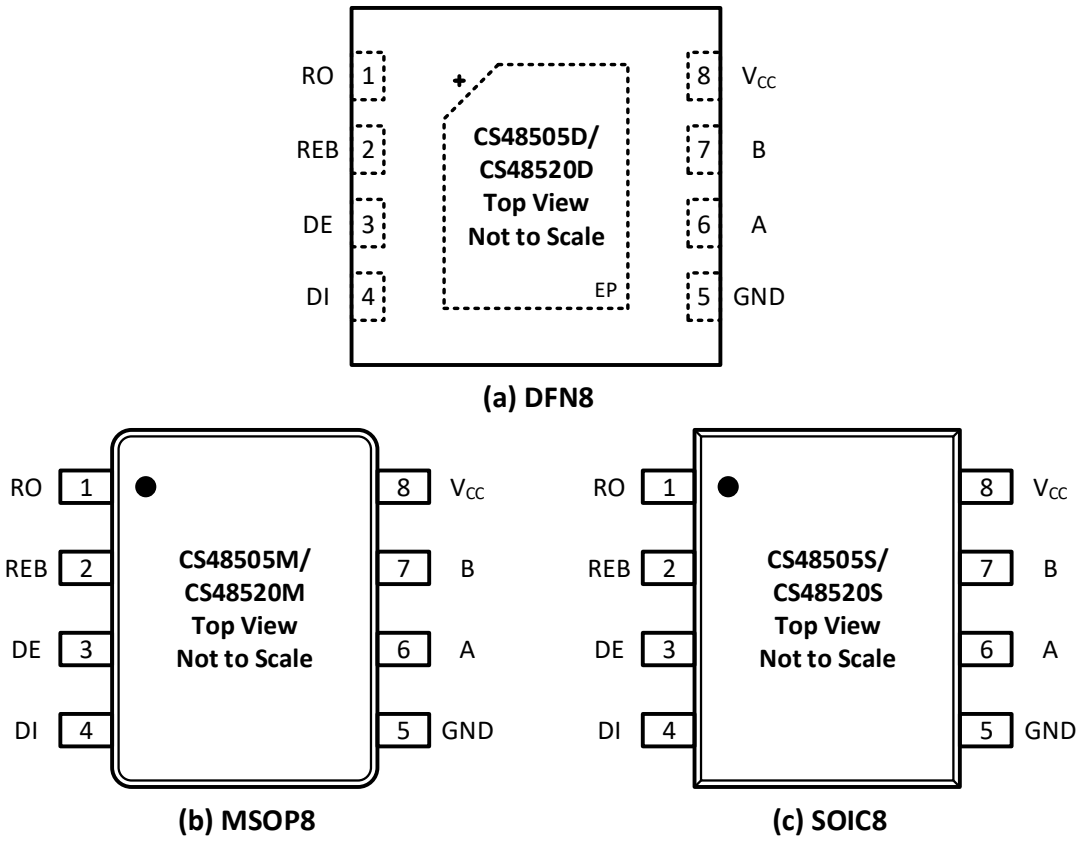


Figure 6-1 CS485xx Pin Configuration

Table 6-1 CS485xx Pin Description and Functions

NAME	PIN NUMBER	TYPE	DESCRIPTION
RO	1	Digital Output	Receiver data output.
REB	2	Digital Input	Receiver enable control, pulled up internally: 1. When REB is low, receiver is enabled; 2. When REB is high or open, receiver is disabled.
DE	3	Digital Input	Driver enable control, pulled down internally: 1. When DE is high, driver is enabled; 2. When DE is low or open, driver is disabled.
DI	4	Digital Input	Driver data input, pulled up internally.
GND	5	Ground	Ground.
A	6	Bus Input/Output	Noninverting driver output/receiver input.
B	7	Bus Input/Output	Inverting driver output/receiver input.
V_{CC}	8	Power	Power supply input, bypass V_{CC} to GND with at least 0.1μF capacitors as close as possible to the device.
EP	--	--	Exposed Pad (DFN8 package only). Connect EP to GND.

7 Specifications

7.1 Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
V_{CC}	Supply voltage[2]	–0.5	7	V
V_{IO}	Bus voltage of A and B[2]	–8	13	V
V_{IO_DIFF}	Differential voltage between A and B	–8	13	V
V_{IO}	Input logical voltage of DI, DE and REB	–0.3	V_{CC} + 0.3[3]	V
V_{IO}	Output logical voltage of RO	–0.3	V_{CC} + 0.3[3]	V
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	–65	150	°C

NOTE:

1. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to the ground terminal (GND) and are peak voltage values.
3. Maximum voltage must not exceed 7V.

7.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Bus pins (A, B) to GND	±20	kV
			All other pins	±8	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins		±2	
		Contact discharge, per IEC 61000-4-2	Bus pins (A, B) to GND	±4	kV
V_{EFT}	Electrical fast transient	Per IEC 61000-4-4	Bus pins (A, B) to GND	±4	

7.3 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage, with respect to GND	3.0	5.0	5.5	V
V_{IN}	Bus input voltage	–7		12	V
V_{IH}	High-level input voltage of DI, DE and REB	2.0		V_{CC}	V
V_{IL}	Low-level input voltage of DI, DE and REB	0		0.8	V
R_L	Differential load resistance	54			Ω
$1/t_{UI}$	Data Rate: CS48505x			0.5	Mbps
$1/t_{UI}$	Data Rate: CS48520x			20	Mbps
T_A	Ambient Temperature	–40		125	°C
T_J	Junction Temperature	–40		150	°C

7.4 Thermal Information

THERMAL METRIC		SOIC8 (S)	MSOP8 (M)	DFN8 (D)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120	160	45	°C/W

7.5 Electrical Characteristics

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{CC} = 5V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\|V_{OD}\|$	Differential output voltage	R_L = 60Ω, –7V ≤ V_{test} ≤ 12V, see Figure 8-1		1.5	3.2		V
		R_L = 60Ω, –7V ≤ V_{test} ≤ 12V, 4.5V ≤ Vcc ≤ 5.5V, see Figure 8-1		2.1	3.2		V
		R_L = 100Ω, C_L = 50pF, see Figure 8-2		1.8	3.6		V
		R_L = 54Ω, C_L = 50pF, see Figure 8-2		1.5	3.2		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential-output voltage	R_L = 100Ω or 54Ω, C_L = 50pF, see Figure 8-2		–50		50	mV
V_{OC}	Common-mode output voltage			1	V_{CC}/2	3.3	V
$\Delta V_{OC(SS)}$	Change in magnitude of common-mode output voltage			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage				450		mV
$\|I_{OS}\|$	Driver short-circuit output current	DE = V_{CC}, –7V ≤ V_O ≤ 12V, or A shorted to B			90	150	mA
Receiver							
I_I	Bus input current	DE = 0V, V_{CC} = 0V or 5.5V	V_I = 12V		70	600	µA
			V_I = –7V	–100	–40		
R_I	Bus input resistance	V_A = –7V, V_B = 12V[1] or V_A = 12V, V_B = –7V[1]		24			kΩ
V_{TH+}	Positive-going receiver input voltage threshold	Over V_{CM} range			–110	–50	mV
$V_{TH–}$	Negative-going receiver input voltage threshold			–200	–140		mV
V_{HYS}[2]	Receiver differential-input voltage threshold hysteresis, $V_{TH+} – V_{TH–}$				30		mV
V_{OH}	High-level output voltage	I_{OH} = –4mA		V_{CC} – 0.5	V_{CC} – 0.3		V
V_{OL}	Low-level output voltage	I_{OL} = 4mA			0.2	0.4	V
I_{OZR}	High-impedance output current	REB = V_{CC}, V_O = 0V or V_{CC}		–1		1	µA
I_{OSR}	Receiver short-circuit output current	REB = DE = 0V, see Figure 8-3				95	mA
Input Logic (DI, DE, REB)							
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{CC}		–5		5	µA
Supply							
I_{CC}	Quiescent supply current	Both driver and receiver enabled, REB = 0V, DE = V_{CC}, empty load, no switching			950	1500	µA
		Driver enabled and receiver disabled, REB = V_{CC}, DE = V_{CC}, empty load, no switching			550	1000	
		Driver disabled and receiver enabled, REB = 0V, DE = 0V, empty load, no switching			700	1100	
		Both driver and receiver disabled, REB = DI = V_{CC}, DE = 0V, empty load, no switching				5	
TSD	Thermal shutdown threshold				200		°C
	Thermal shutdown hysteresis				25		°C

NOTE:

1. The absolute differential voltage between A and B cannot exceed the maximum rated value of 13V. Apply voltage to A and B separately during testing.
2. Under any specific conditions, V_{TH+} is specified to be at least V_{HYS} higher than $V_{TH–}$.

7.6 Timing Characteristics

Over recommended operating temperature range (unless otherwise noted). All typical specifications are at T_A = 25°C and V_{CC} = 5V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver						
t_r, t_f	Differential output rise and fall time	R_L = 54Ω, C_L = 50pF, see Figure 8-4		5	12	ns
t_{PHL}, t_{PLH}	Driver propagation delay			5	12	ns
$t_{SK(P)}$	Driver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				3.5	ns
t_{PHZ}, t_{DLZ}	Driver disable time	See Figure 8-5 and Figure 8-6		10	30	ns
t_{PZH}, t_{PZL}	Driver enable time[1]	REB = 0V, see Figure 8-5 and Figure 8-6		10	30	ns
		REB = V_{CC}, see Figure 8-5 and Figure 8-6		6	12	μs
Receiver						
t_r, t_f	Receiver output rise and fall time	C_L = 15pF[2], see Figure 8-7		4	8	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time			40	80	ns
$t_{SK(P)}$	Receiver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				4	ns
t_{PHZ}, t_{PLZ}	Receiver disable time	See Figure 8-8		7	20	ns
t_{PZH}, t_{PZL}	Receiver enable time[3]	DE = V_{CC}, see Figure 8-8 and Figure 8-9		30	70	ns
		DE = 0V, see Figure 8-8 and Figure 8-9		6	12	μs

NOTE:

1. When DE and REB are shorted together, driver enable time refers to the case when REB = 0V.
2. C_L includes probe and fixture capacitance.
3. When DE and REB are shorted together, receiver enable time refers to the case when DE = V_{CC}.

7.7 Typical Characteristics

All typical specifications are at T_A = 25°C and V_{CC} = 5V (unless otherwise noted).

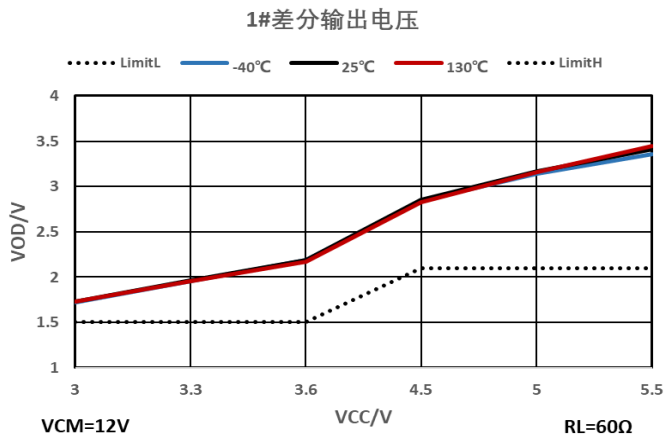


Figure 7-1 Driver Differential Output Voltage @ V_{CM} = 12V

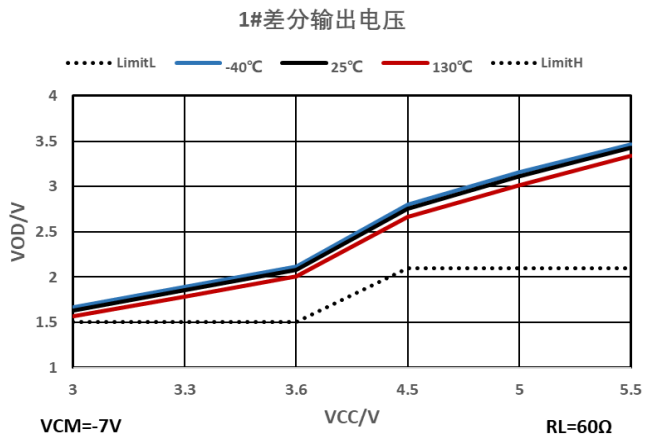


Figure 7-2 Driver Differential Output Voltage @ V_{CM} = -7V

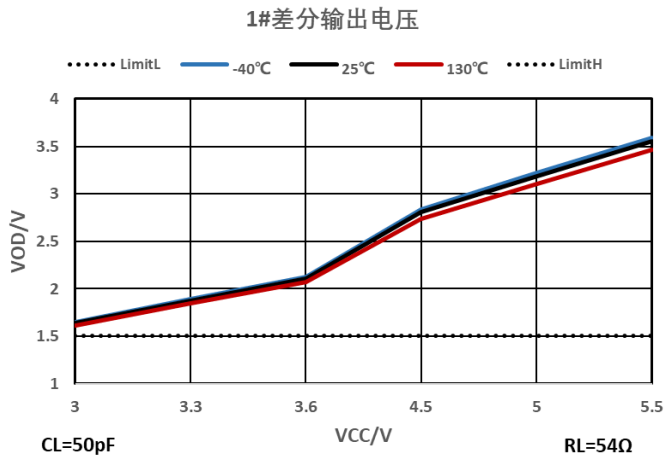


Figure 7-3 Driver Differential Output Voltage with 54Ω Load

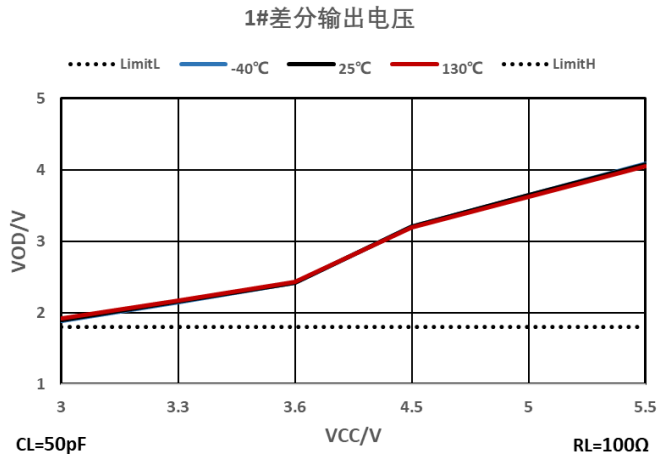


Figure 7-4 Driver Differential Output Voltage with 100Ω Load

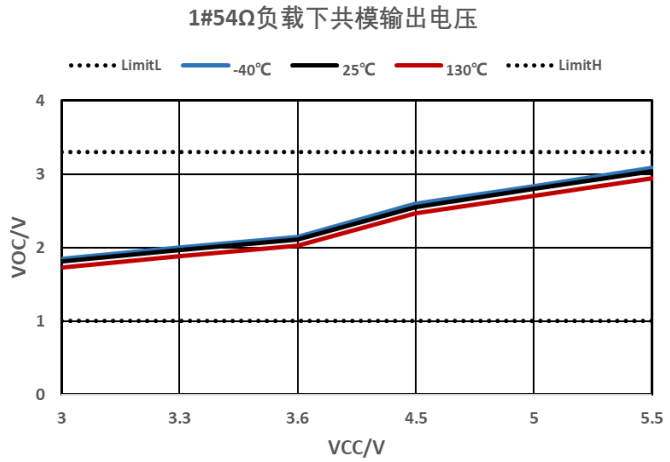


Figure 7-5 Driver Common-mode Output Voltage with 54Ω Load

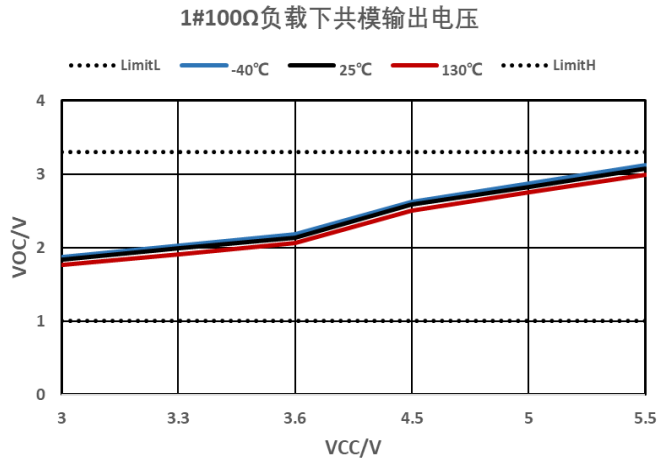


Figure 7-6 Driver Common-mode Output Voltage with 100Ω Load

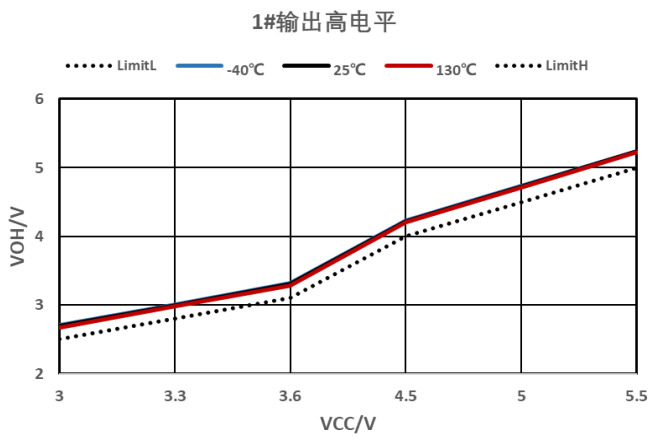


Figure 7-7 Receiver Output @ Logic-high

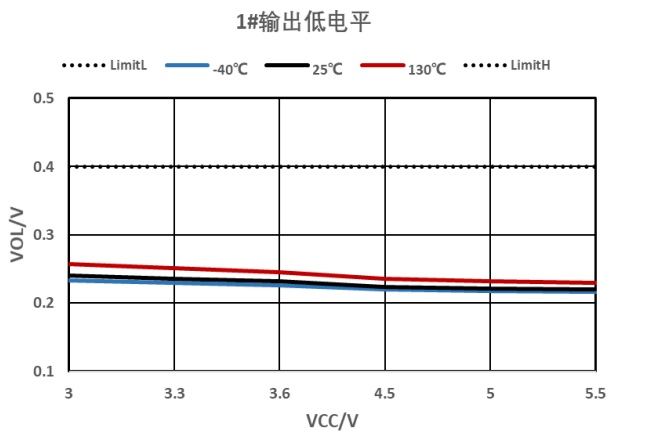


Figure 7-8 Receiver Output @ Logic-low

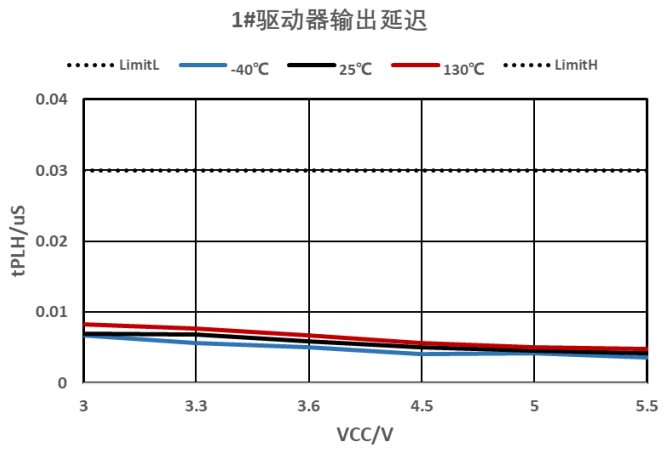


Figure 7-9 Driver Propagation Delay vs. Supply Voltage (L to H)

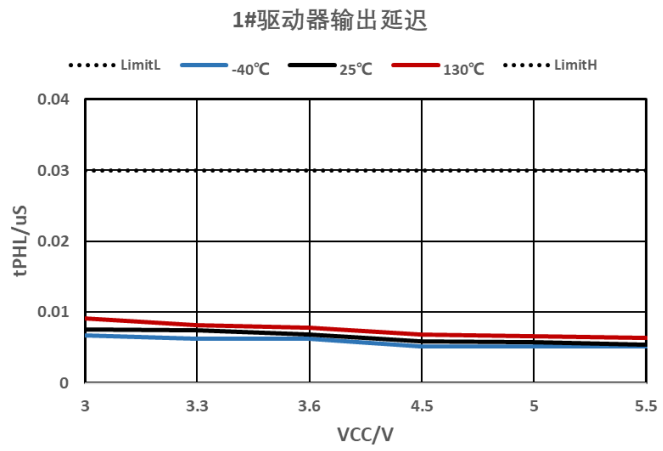


Figure 7-10 Driver Propagation Delay vs. Supply Voltage (H to L)

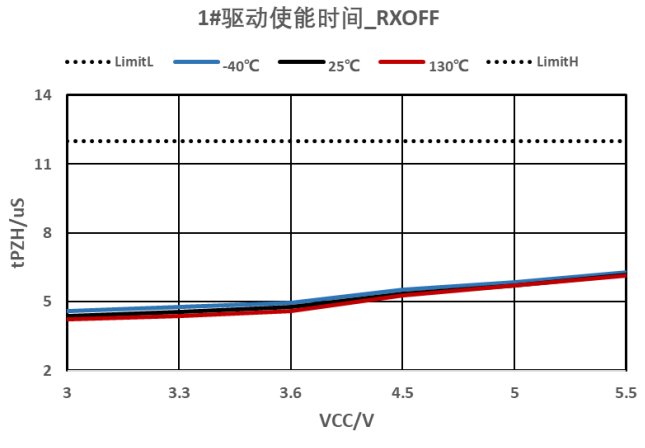


Figure 7-11 Driver Enable Time vs. Supply Voltage: t_{PZH}

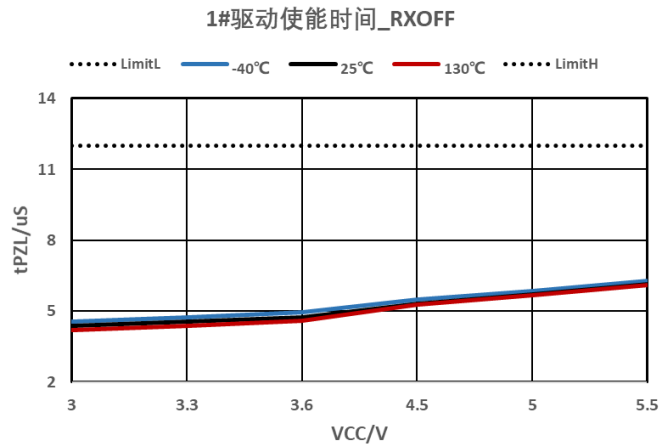


Figure 7-12 Driver Enable Time vs. Supply Voltage: t_{PZL}

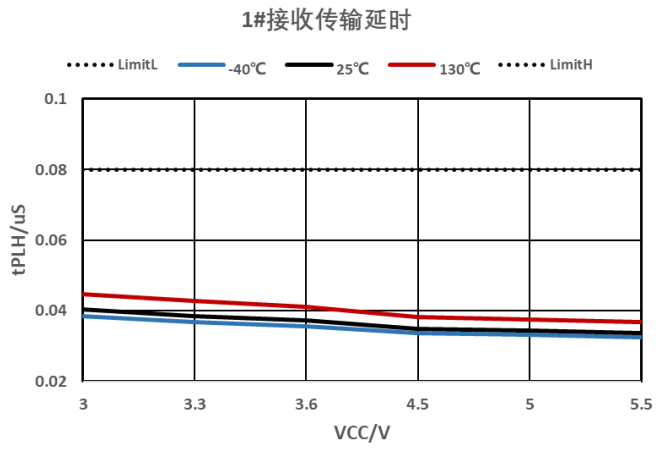


Figure 7-13 Receiver Propagation Delay vs. Supply Voltage (L to H)

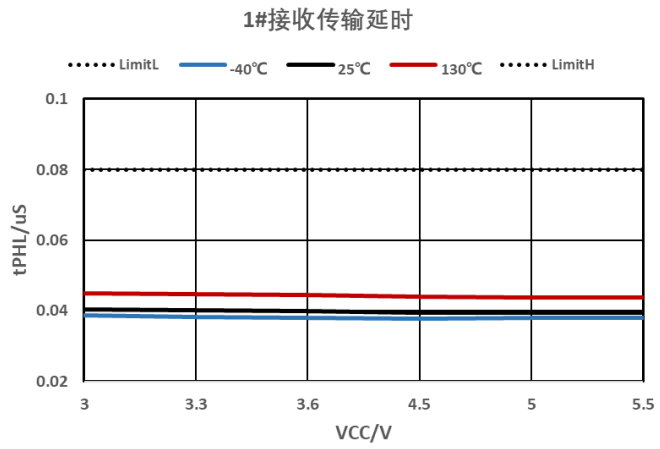


Figure 7-14 Receiver Propagation Delay vs. Supply Voltage (H to L)

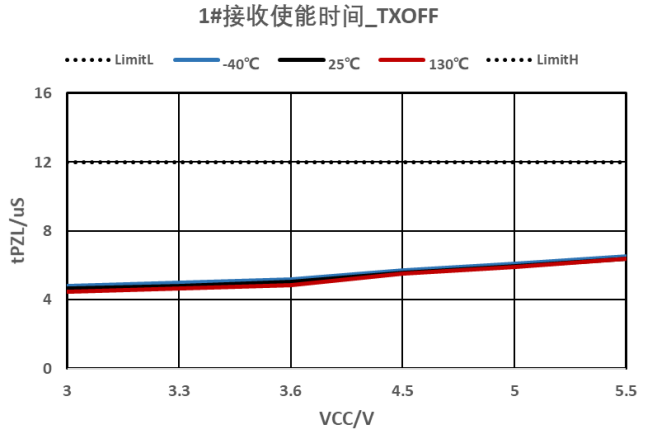


Figure 7-15 Receiver Enable Time vs. Supply Voltage: t_{PZL}

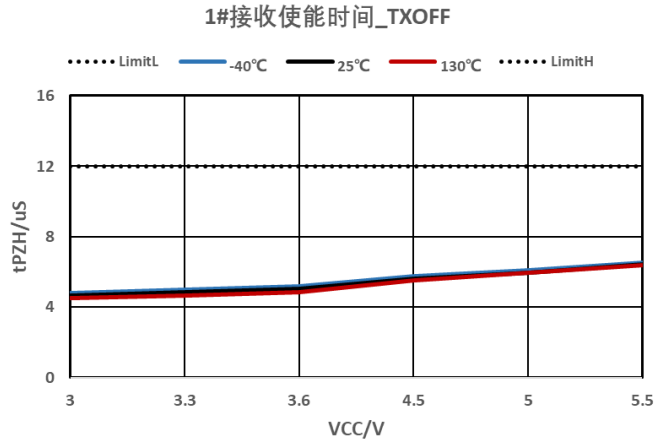


Figure 7-16 Receiver Enable Time vs. Supply Voltage: t_{PZH}

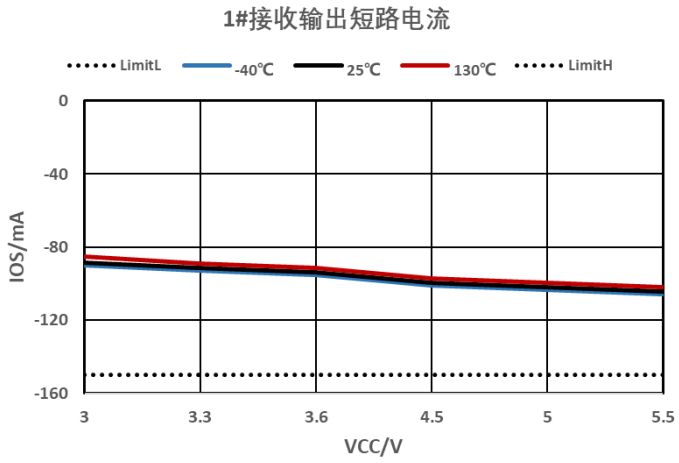


Figure 7-17 Receiver Output Short Current

8 Parameter Measurement Information

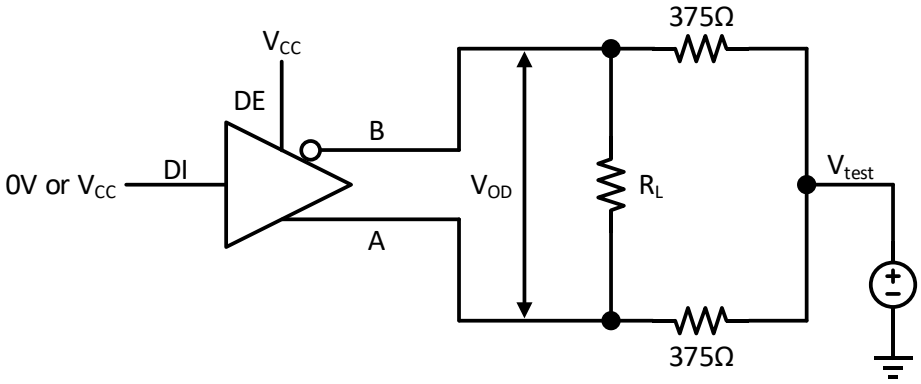


Figure 8-1 Measurement of Driver Differential Output Voltage With Common-Mode Load

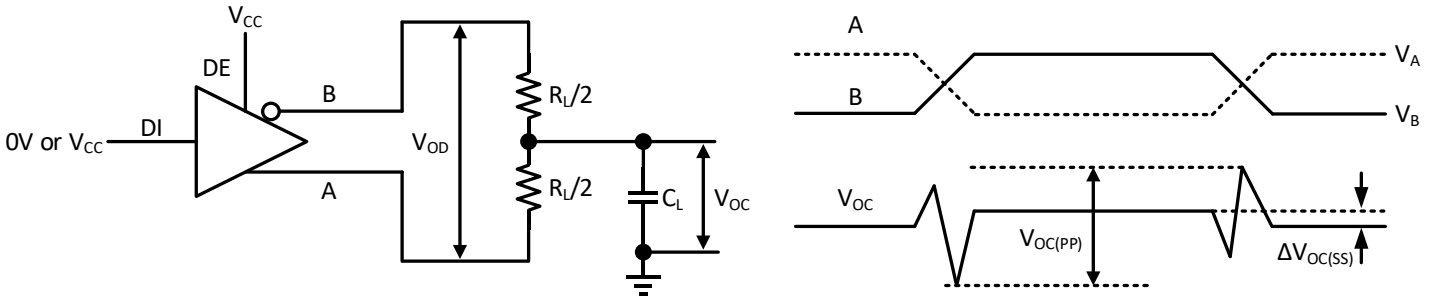


Figure 8-2 Measurement of Driver Differential and Common-Mode Output Voltage With RS-485 Load

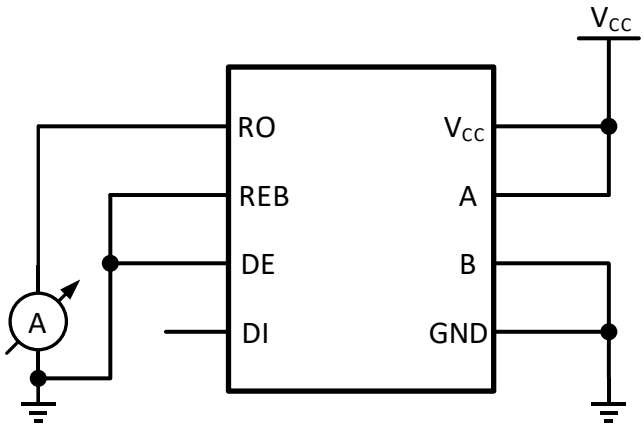


Figure 8-3 Measurement of Receiver Output Short Circuit Current

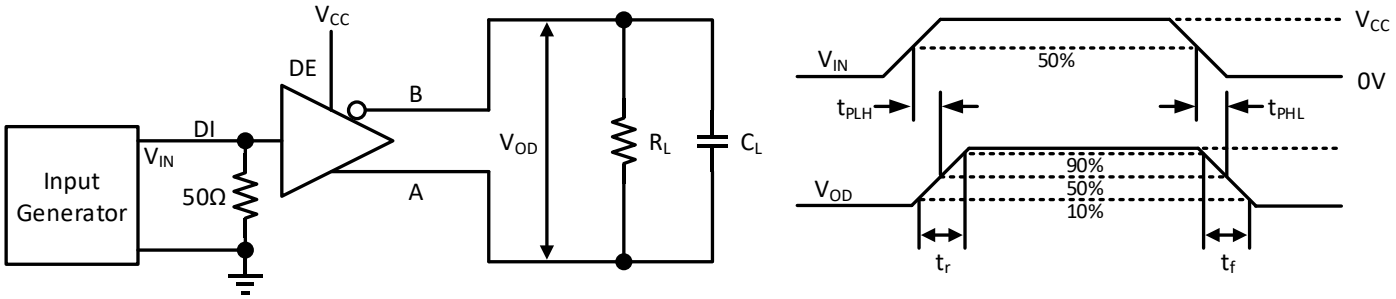


Figure 8-4 Measurement of Driver Output Rise and Fall Time and Propagation Delay

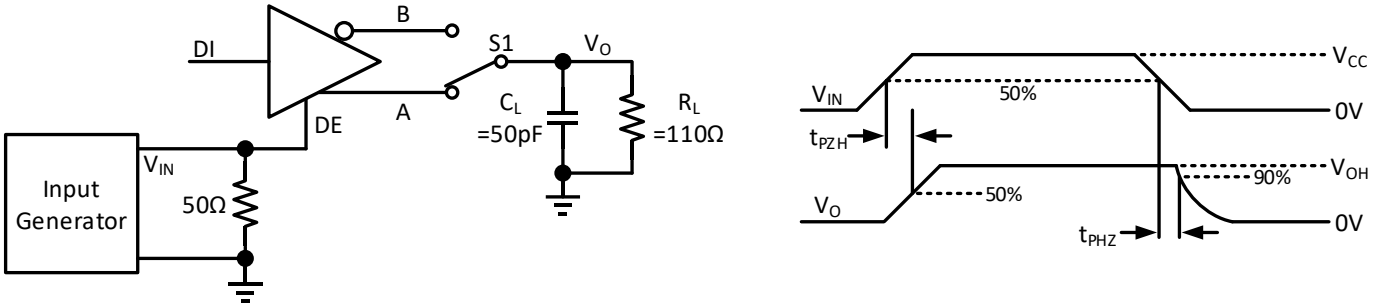


Figure 8-5 Measurement of Driver Enable and Disable Time With Active High Output and Pull-Down Load

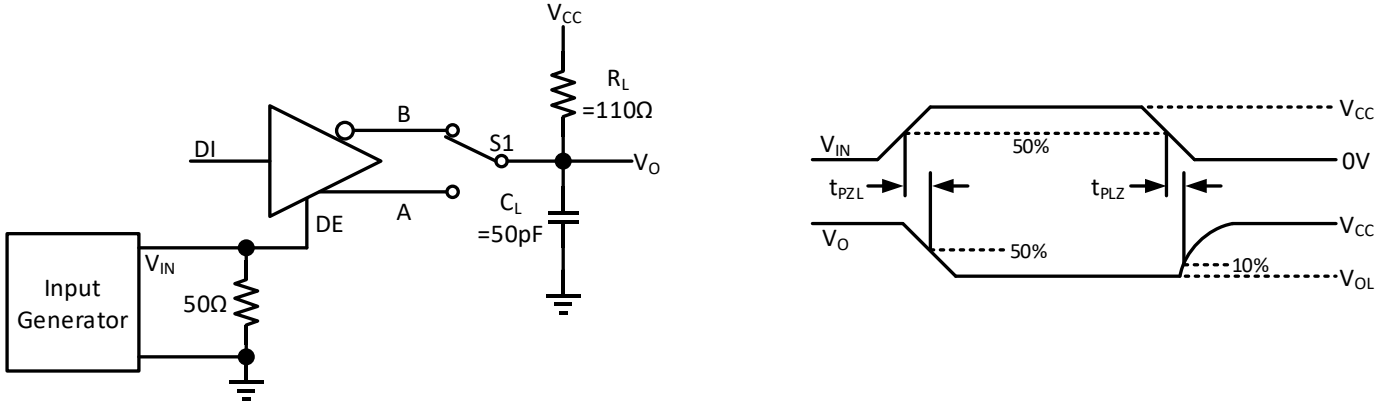


Figure 8-6 Measurement of Driver Enable and Disable Time With Active Low Output and Pull-Up Load

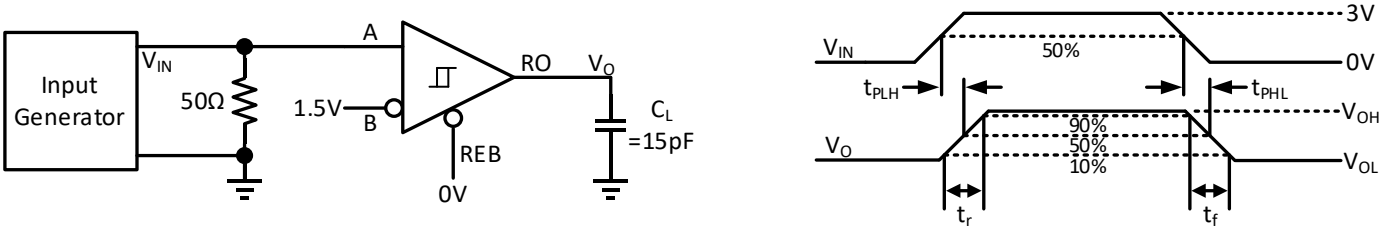


Figure 8-7 Measurement of Receiver Output Rise and Fall Time and Propagation Delay

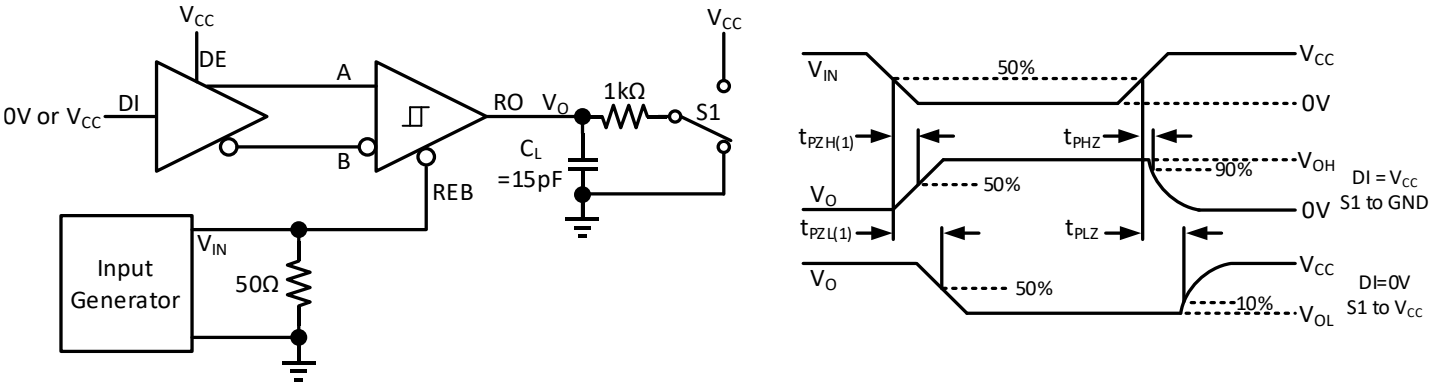


Figure 8-8 Measurement of Receiver Enable/Disable Time With Driver Enabled

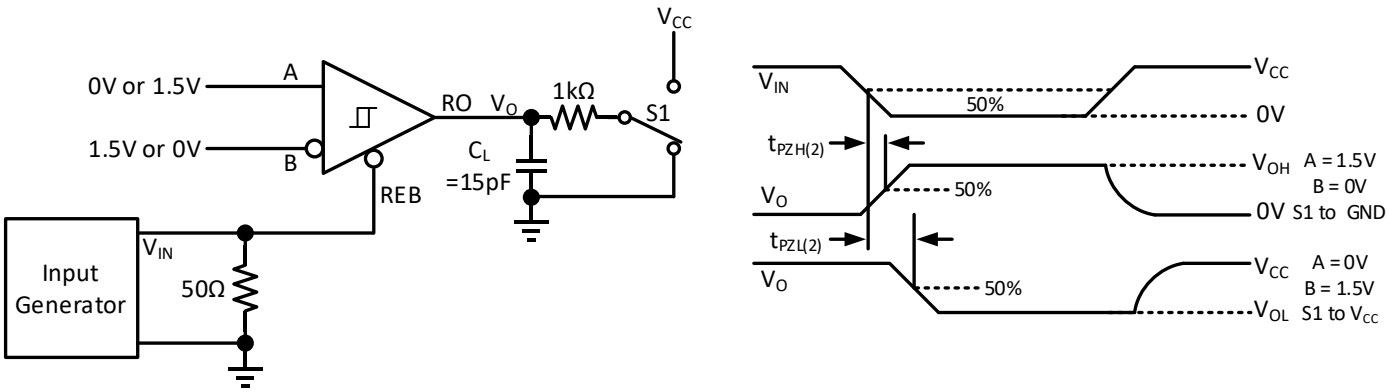


Figure 8-9 Measurement of Receiver Enable Time With Driver Disabled

9 Detailed Description

9.1 System Overview

The CS485xx devices are optimized for RS-485 applications which meet or exceed the requirements of the TIA/EIA-485A standard. These devices have two options in data rate: 500kbps and 20Mbps. The bus pins could withstand high-level ESD events to protect internal circuit without damage, which is suitable in harsh industrial and electrical environments. These devices could guarantee a logical high on the receiver output when the bus inputs are open, short or on idle state, thus eliminating the need of external failsafe bias resistors. These devices also integrate thermal shutdown protection circuit. When the junction temperature rises above 170°C (typical value), the output of driver is disabled and the output of RO is high-impedance. When the junction temperature falls below 150°C (typical value), the output of both driver and receiver is re-enabled. These devices are specified over extended industrial temperature range of –40°C to 125°C.

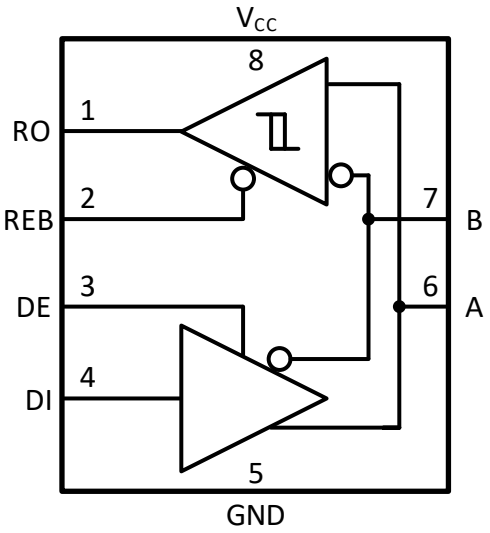


Figure 9-1 Simplified Functional Blcok Diagram

9.2 Device Function Mode

9.2.1 Driver

Table 9-1 Truth Table of Driver[1]

INPUT	ENABLE	OUTPUT		FUNCTION
DI[2]	DE[3]	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	High-Z	High-Z	Driver disabled
X	Open	High-Z	High-Z	Driver disabled by default
Open	H	H	L	Actively drive bus high by default

NOTE:
1. H = high level, L = low level, X = irrelevant, High-Z = high impedance.
2. DI is weakly pulled up to V_{CC} internally.
3. DE is weakly pulled down to GND internally.

When the enable pin DE of driver is logical high, the differential outputs of A and B follow with the data input DI, which is shown in Table 9-1.

When DE is logical low or open, the driver is disabled, the outputs of A and B are high-impedance and are irrelevant to the state at DI pin. DI pin is weakly pulled up to V_{CC} internally, the output of A is high while B is low when driver is enabled and DI's input is open.

9.2.2 Receiver

When the enable pin REB of receiver is logical low, receiver is enabled. The truth table of receiver is shown in Table 9-2.

When the bus differential input voltage V_{ID} is greater than or equal to V_{TH+}, receiver output RO is logical high. When V_{ID} is less than or equal to V_{TH-}, receiver output RO is logical low. When V_{ID} is between V_{TH+} and V_{TH-}, receiver output RO is indeterminate.

When REB is logical high or open, the receiver output RO is high-impedance and is irrelevant to the magnitude and polarity of V_{ID}.

When the bus inputs are open, short or on idle state, a failsafe logic high output at RO pin is achieved, avoiding indeterminate state which may result in system communication errors.

Table 9-2 Truth Table of Receiver[1]

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	REB[2]	RO	
$V_{ID} \geq V_{TH+}$	L	H	Output valid high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} \leq V_{TH-}$	L	L	Output valid low
X	H	High-Z	Receiver disabled
X	Open	High-Z	Receiver disabled by default
Open-circuit bus	L	H	Failsafe output high
Short-circuit bus	L	H	Failsafe output high
Idle (terminated) bus	L	H	Failsafe output high

NOTE:

1. H = high level, L = low level, X = irrelevant, High-Z = high impedance, Open = no connection, ? = indeterminate.
2. REB is weakly pulled up to V_{CC} internally.

10 Application and Implementation

10.1 Typical Application

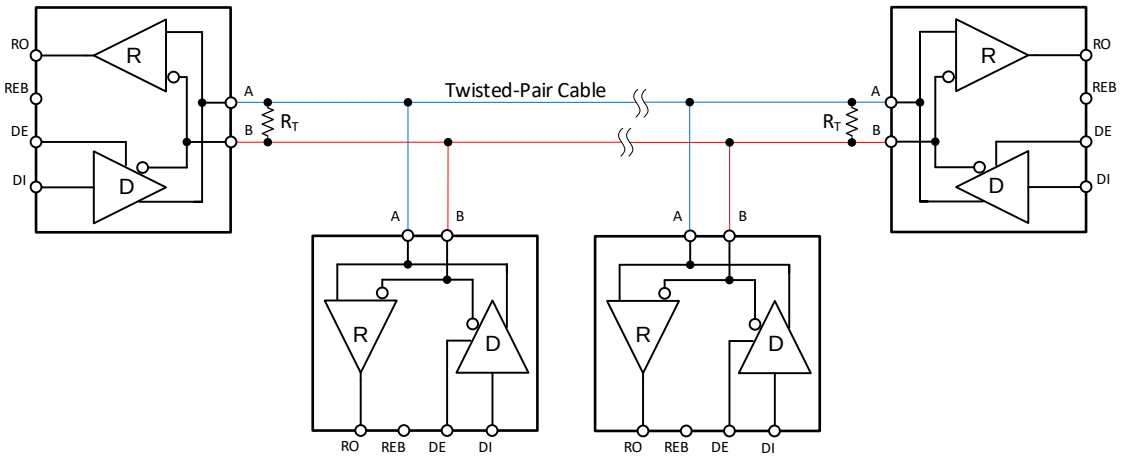


Figure 10-1 Typical RS-485 Network

The typical RS-485 network consists of multiple transceivers connecting in parallel to a bus cable. To eliminate the line reflection, both ends of the cable terminate a termination resistor R_T which should be matched to the characteristic impedance Z_O of the cable. At the same time, please keep the stub lengths off the main line as short as possible. This parallel termination method could achieve higher data rates over longer cable length. The typical RS-485 network utilizing CS485xx is shown in Figure 10-1.

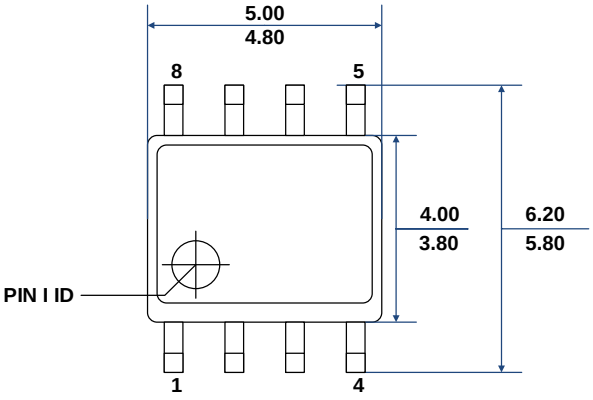
10.2 Power Supply Recommendation

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with 100nF to 220nF ceramic capacitors located as close as possible to the supply pins. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes. At the same time, please keep the voltage in V_{CC} pin with respect to GND pin is below 5.5V.

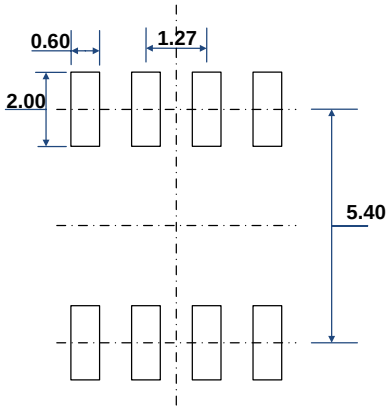
11 Package Information

11.1 SOIC8 (S) Package

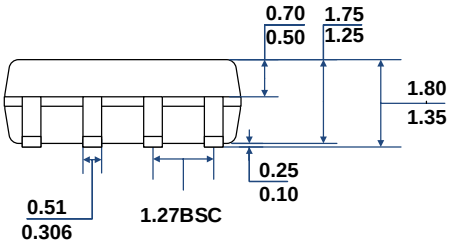
The values for the dimensions are shown in millimeters.



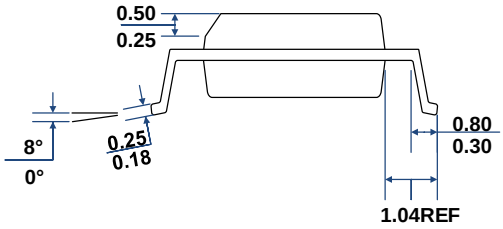
TOP VIEW



RECOMMENDED LAND PATTERN



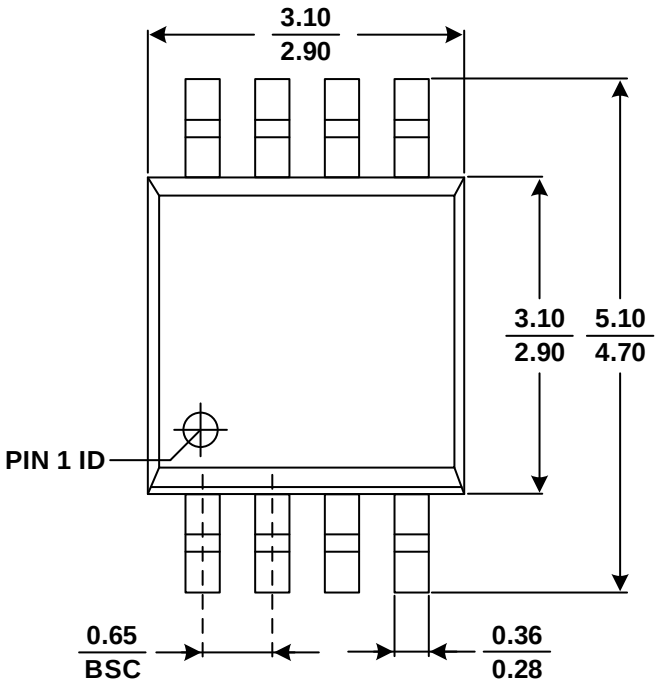
FRONT VIEW



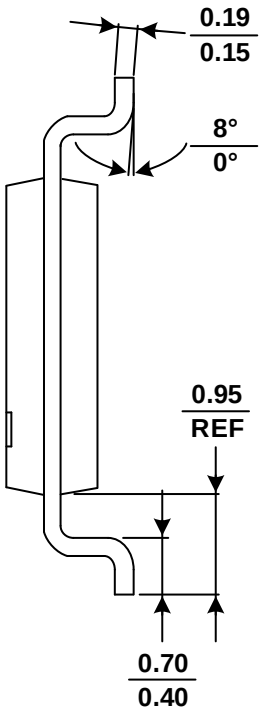
LEFT-SIDE VIEW

11.2 MSOP8 (M) Package

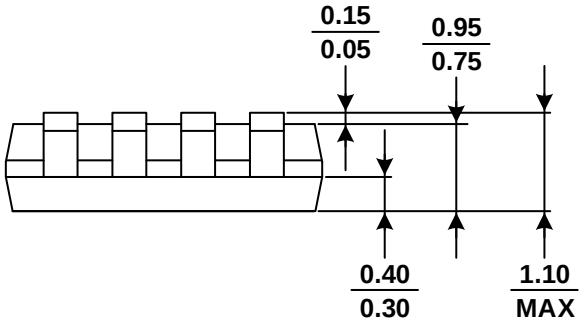
The values for the dimensions are shown in millimeters.



TOP VIEW



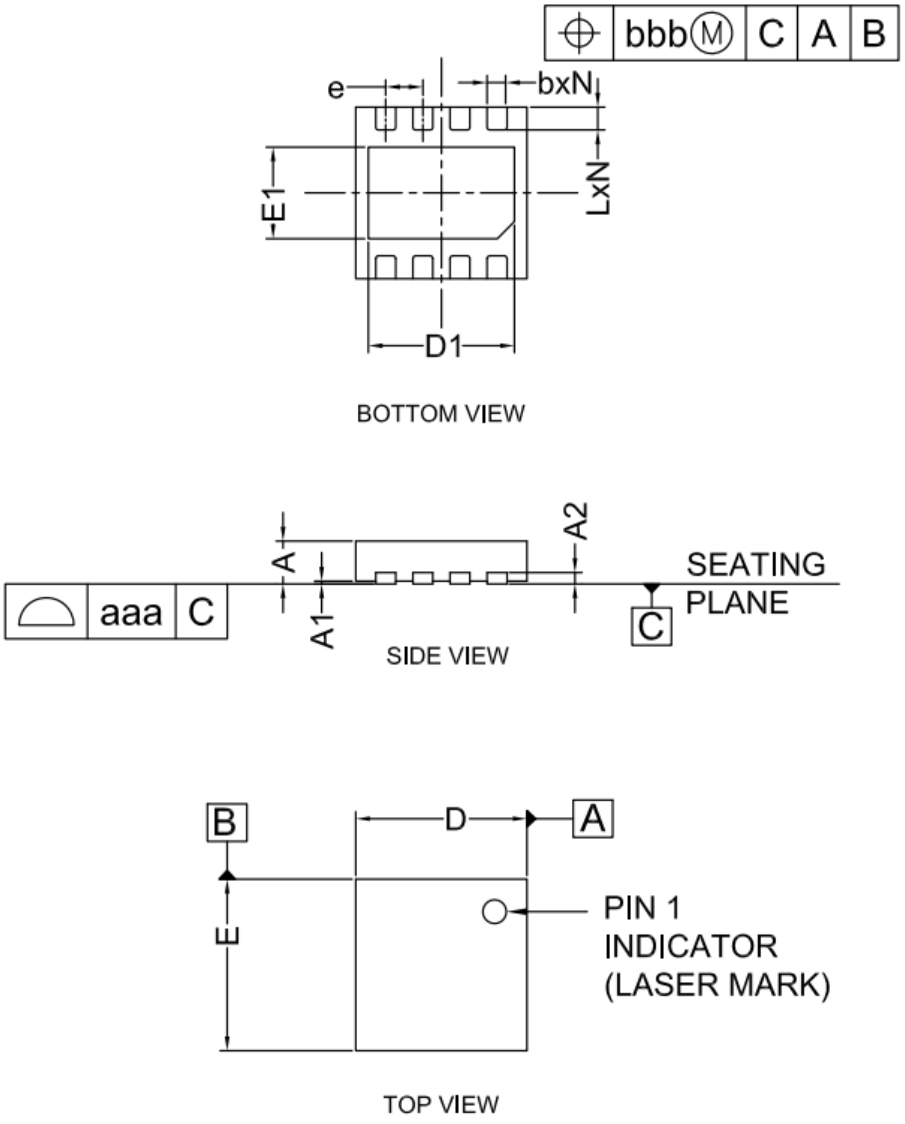
SIDE VIEW



SIDE VIEW

11.3 DFN8 (D) Package

The values for the dimensions are shown in millimeters.



SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.203	
b	0.30	0.35	0.40
D	2.90	3.00	3.10
D1	2.51	2.56	2.61
E	2.90	3.00	3.10
E1	1.55	1.60	1.65
e		0.65BSC	
L	0.35	0.40	0.45
N		8	
aaa		0.08	
bbb		0.10	

12 Soldering Information

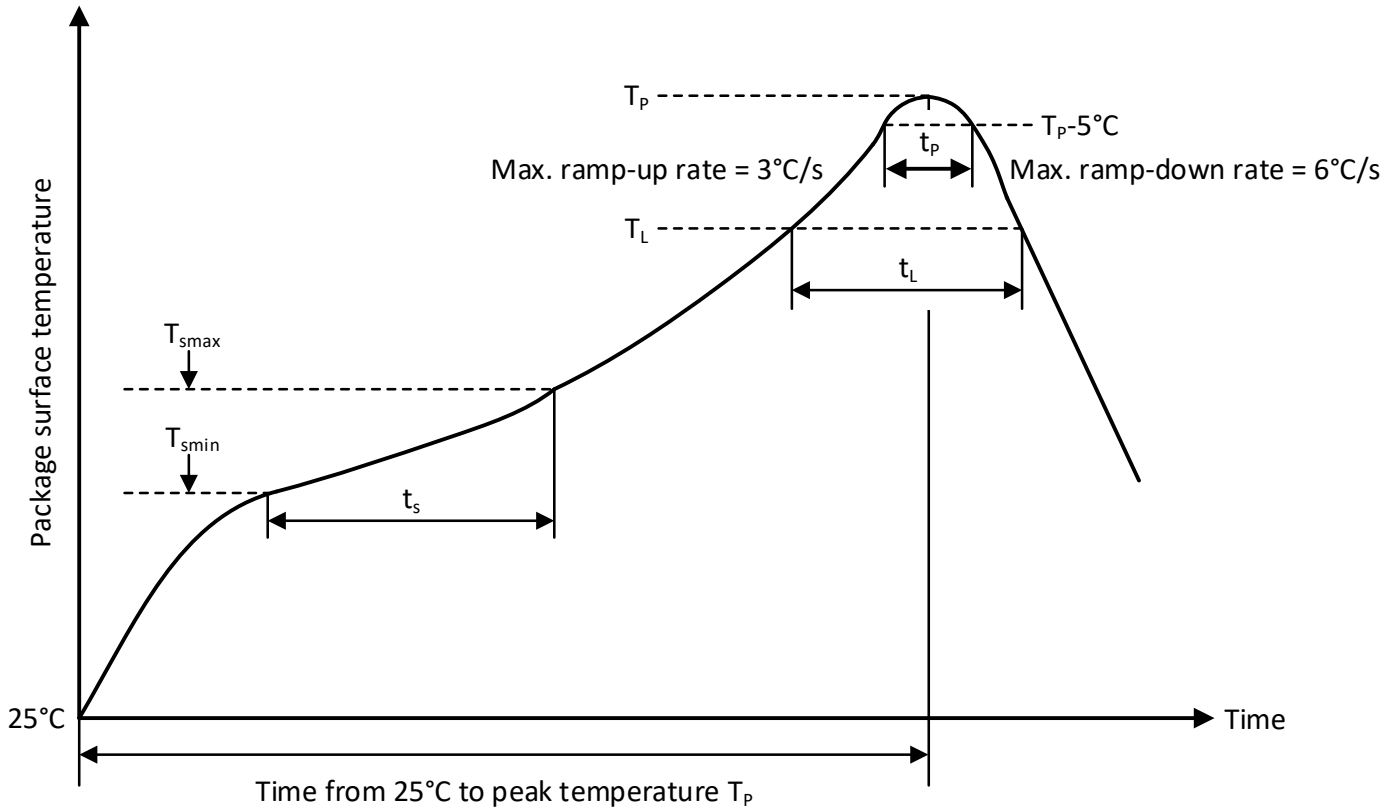


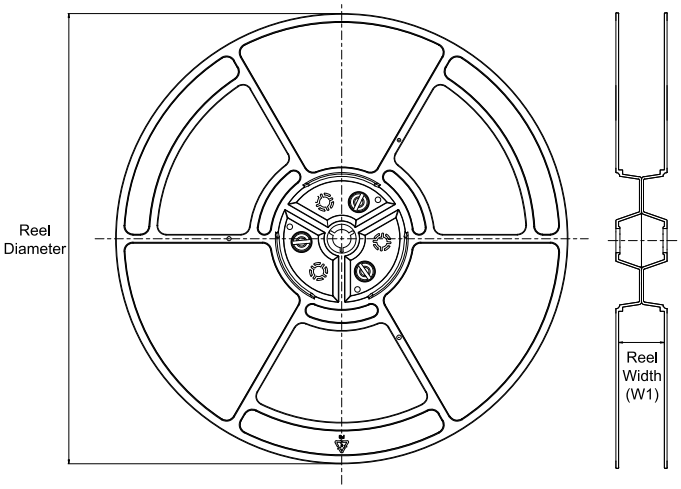
Figure 12-1 Soldering Temperature Curve

Table 12-1 Soldering Temperature Parameters

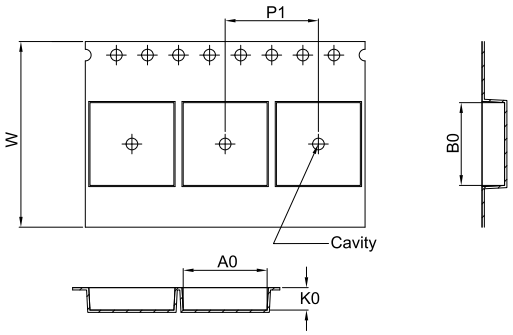
Profile Feature	Pb-Free Soldering
Ramp-up rate (T_L = 217°C to peak T_P)	3°C/s max
Time t_s of preheat temp (T_{smin} = 150°C to T_{smax} = 200°C)	60~120 seconds
Time t_L to be maintained above 217°C	60~150 seconds
Peak temperature T_P	260°C
Time t_P within 5°C of actual peak temp	30 seconds max
Ramp-down rate (peak T_P to T_L = 217°C)	6°C/s max
Time from 25°C to peak temperature T_P	8 minutes max

13 Tape and Reel Information

REEL DIMENSIONS

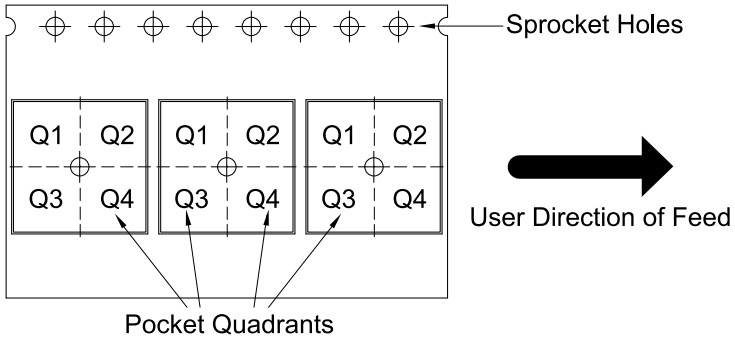


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CS48505S	SOIC8	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CS48520S	SOIC8	S	8	2500	330	12.4	6.5	5.4	2.1	8.0	12.0	Q1
CS48505M	MSOP8	M	8	5000	330	12.6	6.55	5.4	1.9	8.0	12.0	Q1
CS48520M	MSOP8	M	8	5000	330	12.6	6.55	5.4	1.9	8.0	12.0	Q1
CS48505D	DFN8	D	8	3000	330	12.4	3.3	3.3	1.1	8.0	12.0	Q1
CS48520D	DFN8	D	8	3000	330	12.4	3.3	3.3	1.1	8.0	12.0	Q1

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